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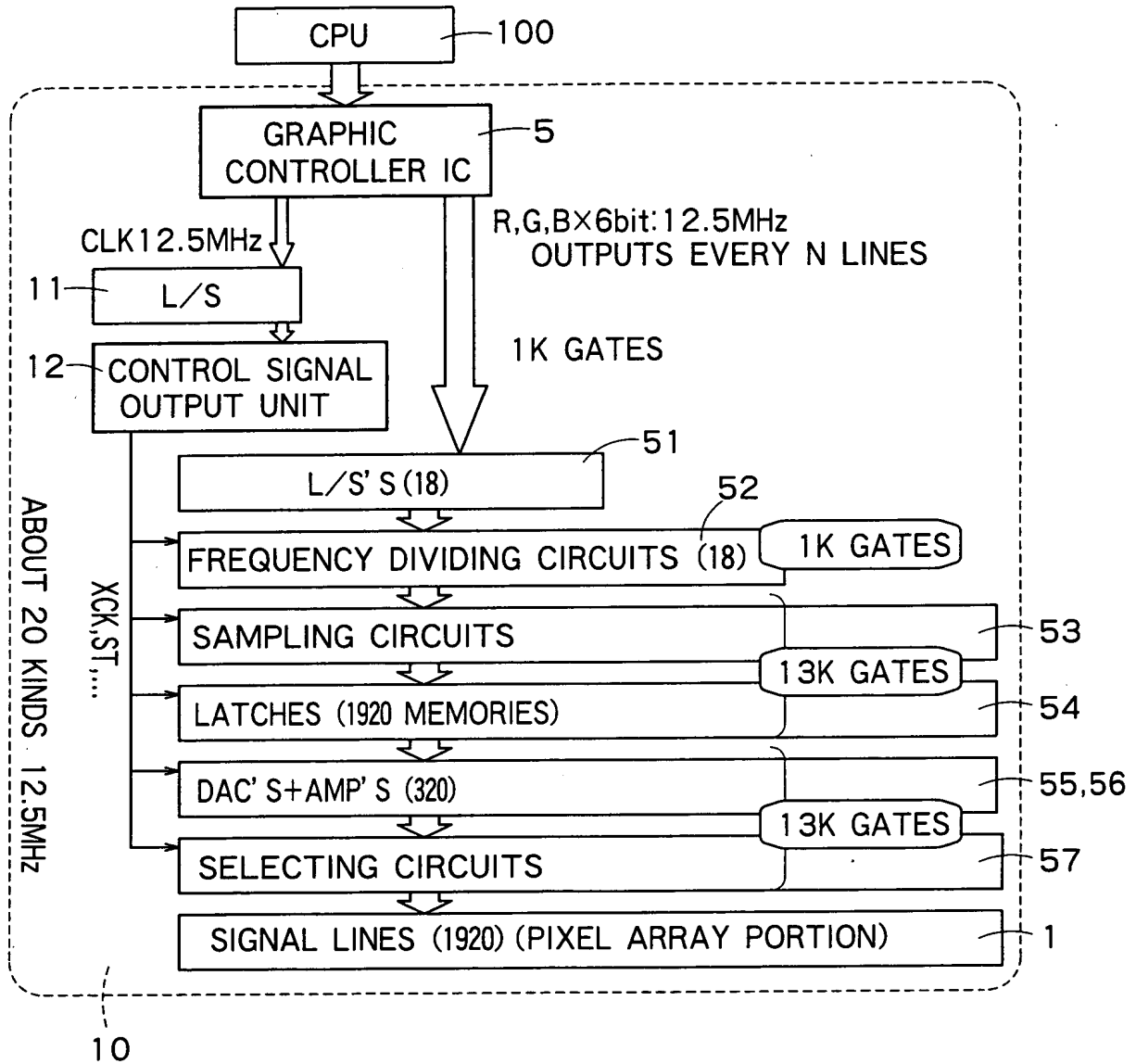


FIG. 1

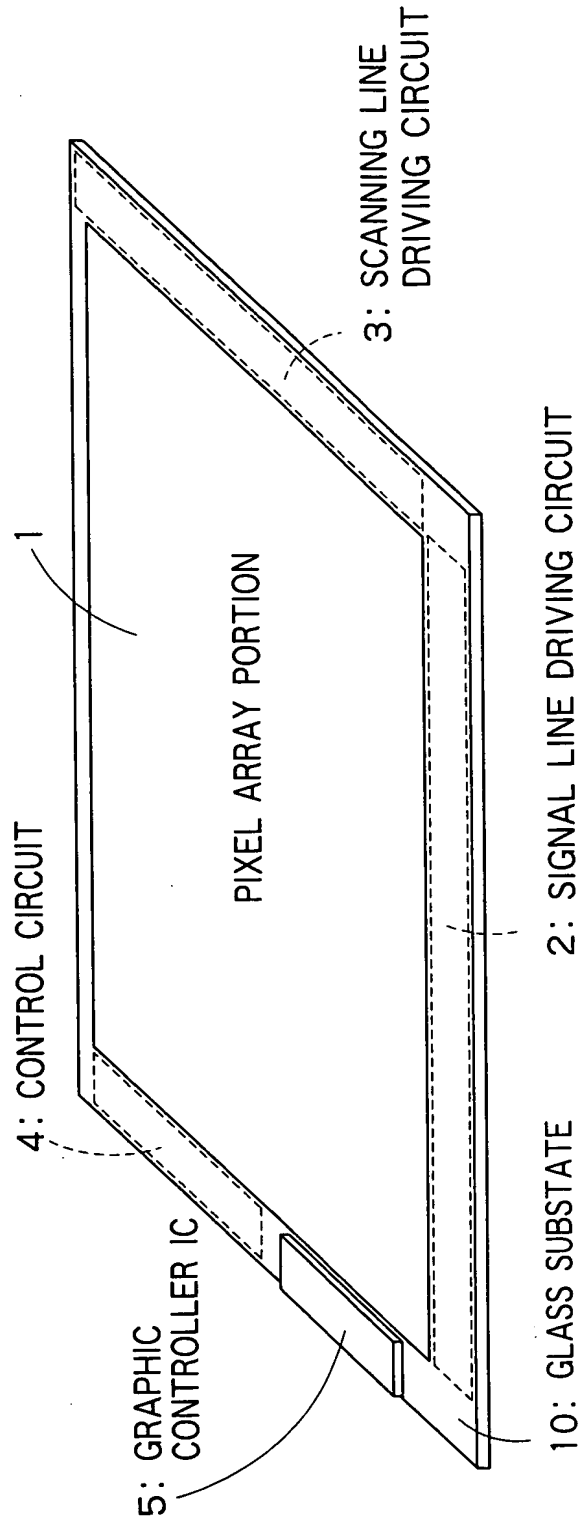
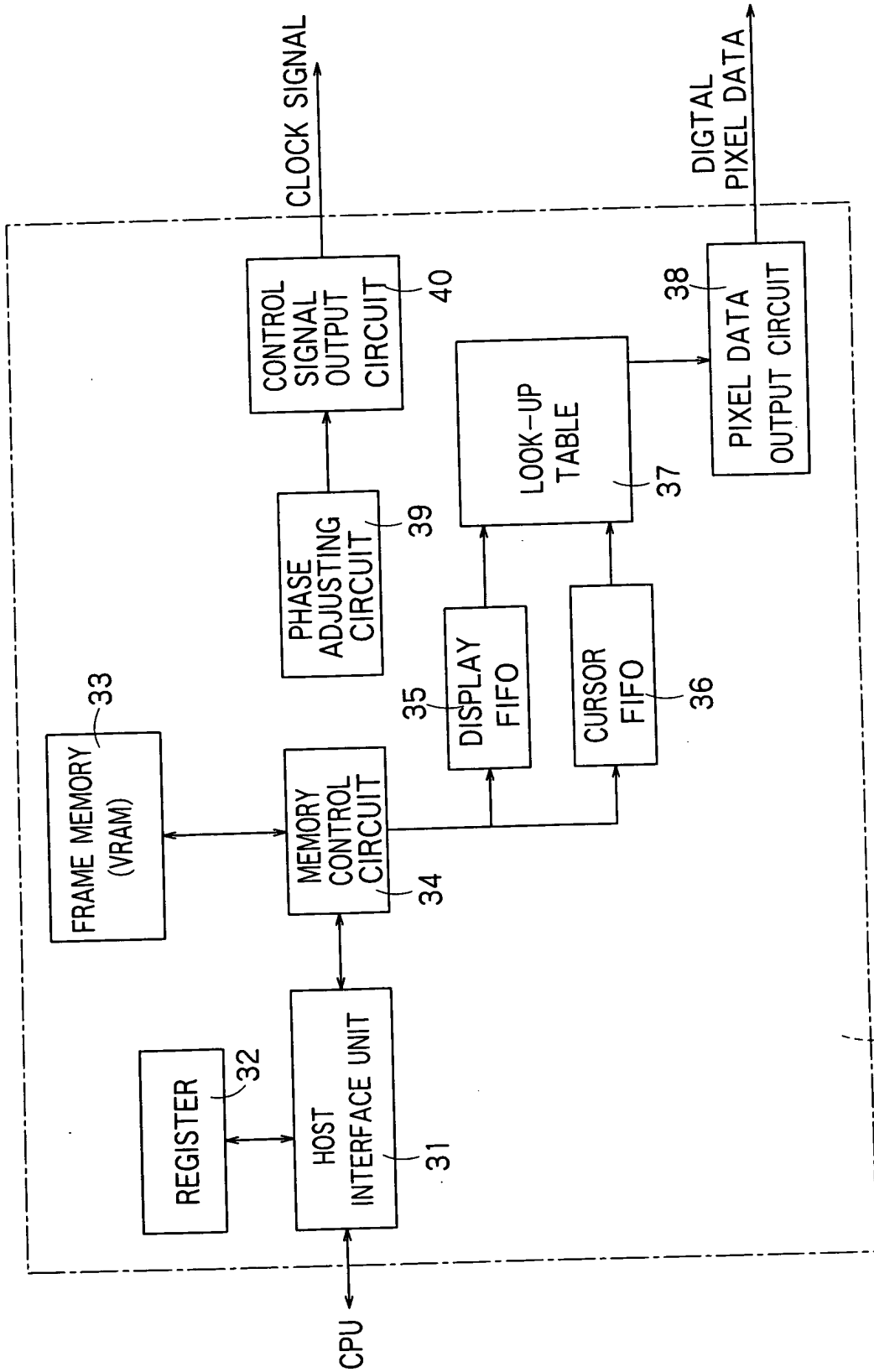


FIG. 2

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5: GRAPHIC CONTROLLER IC

FIG. 3

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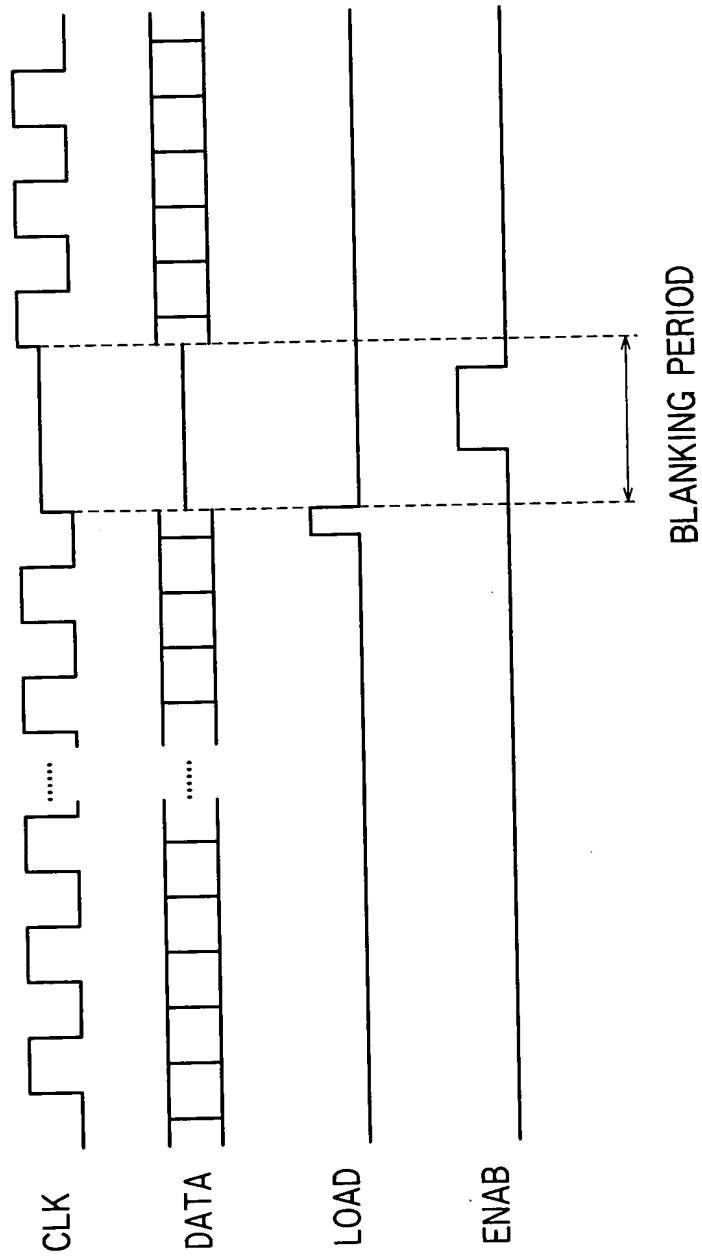


FIG. 4

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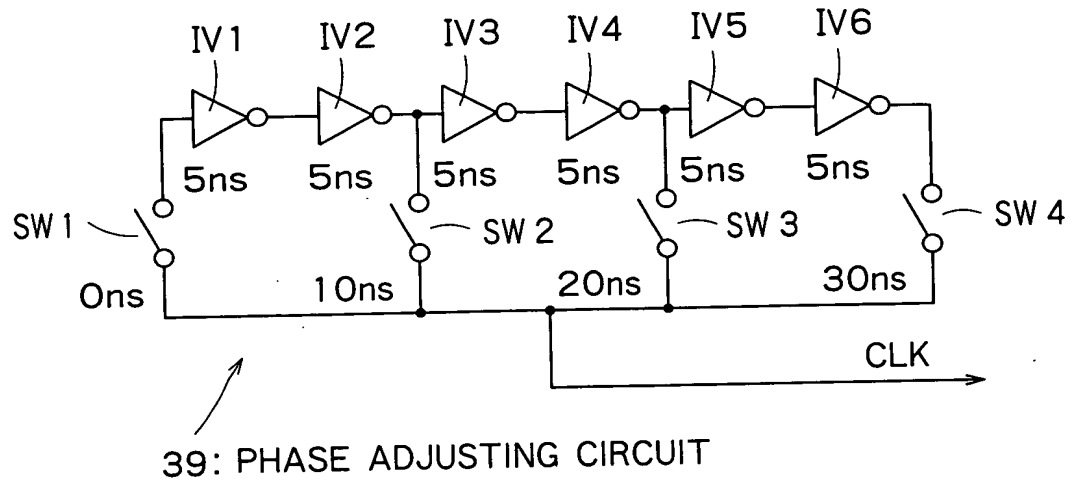


FIG. 5

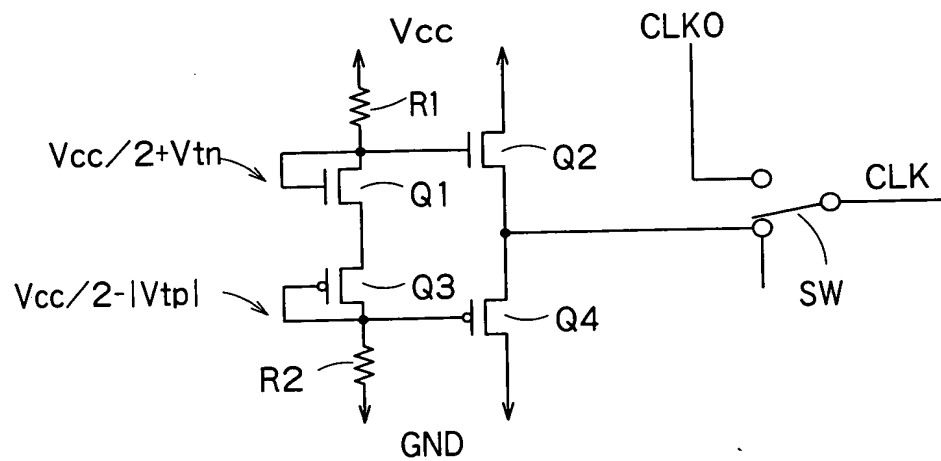


FIG. 6

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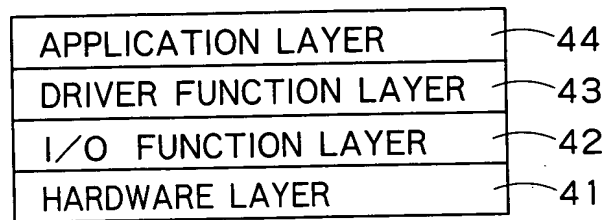


FIG. 7

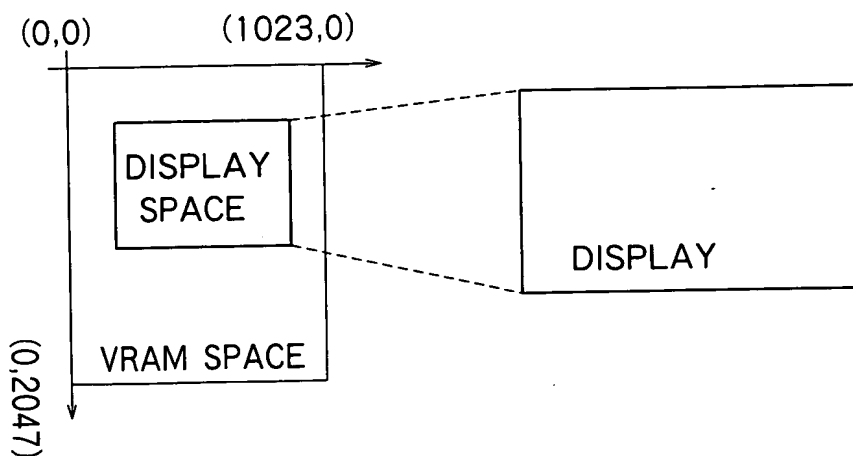


FIG. 8

09842800-042701

2: SIGNAL LINE DRIVING CIRCUIT

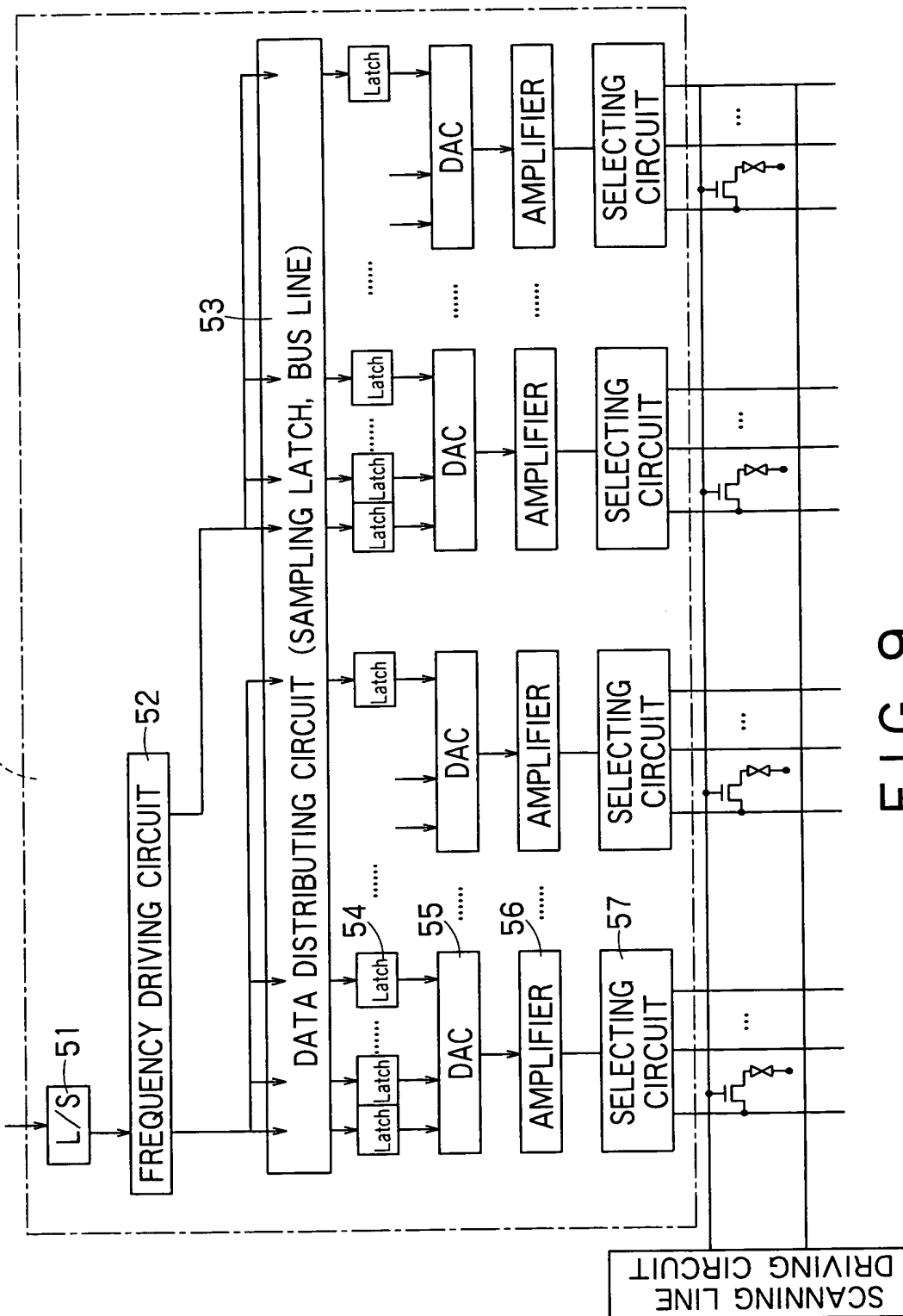


FIG. 9

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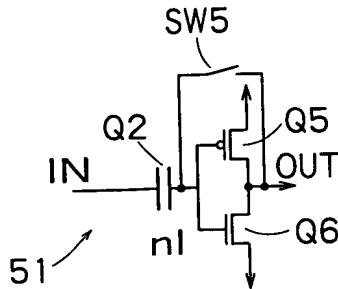


FIG. 10

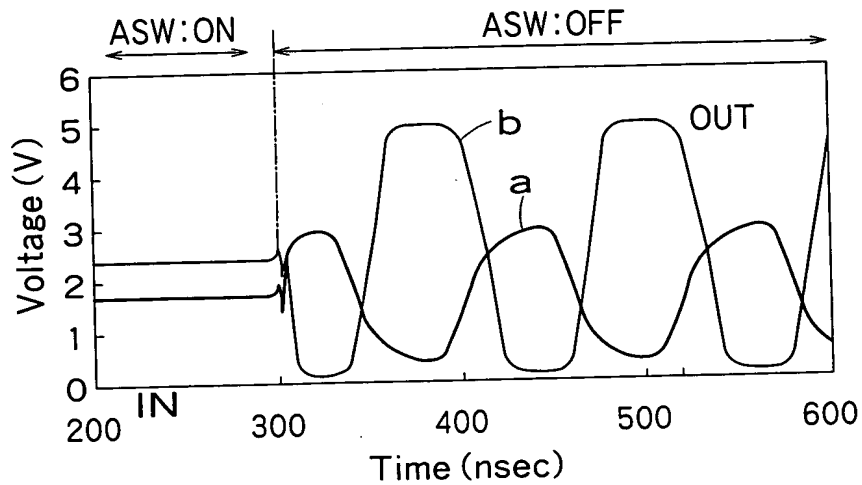


FIG. 11

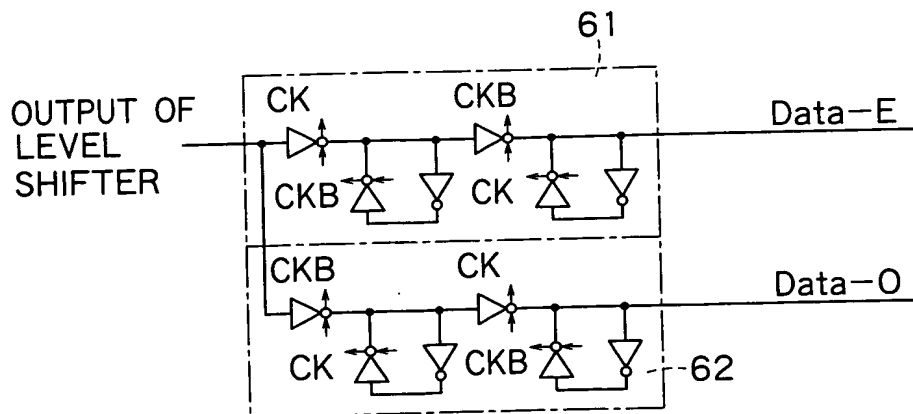


FIG. 12

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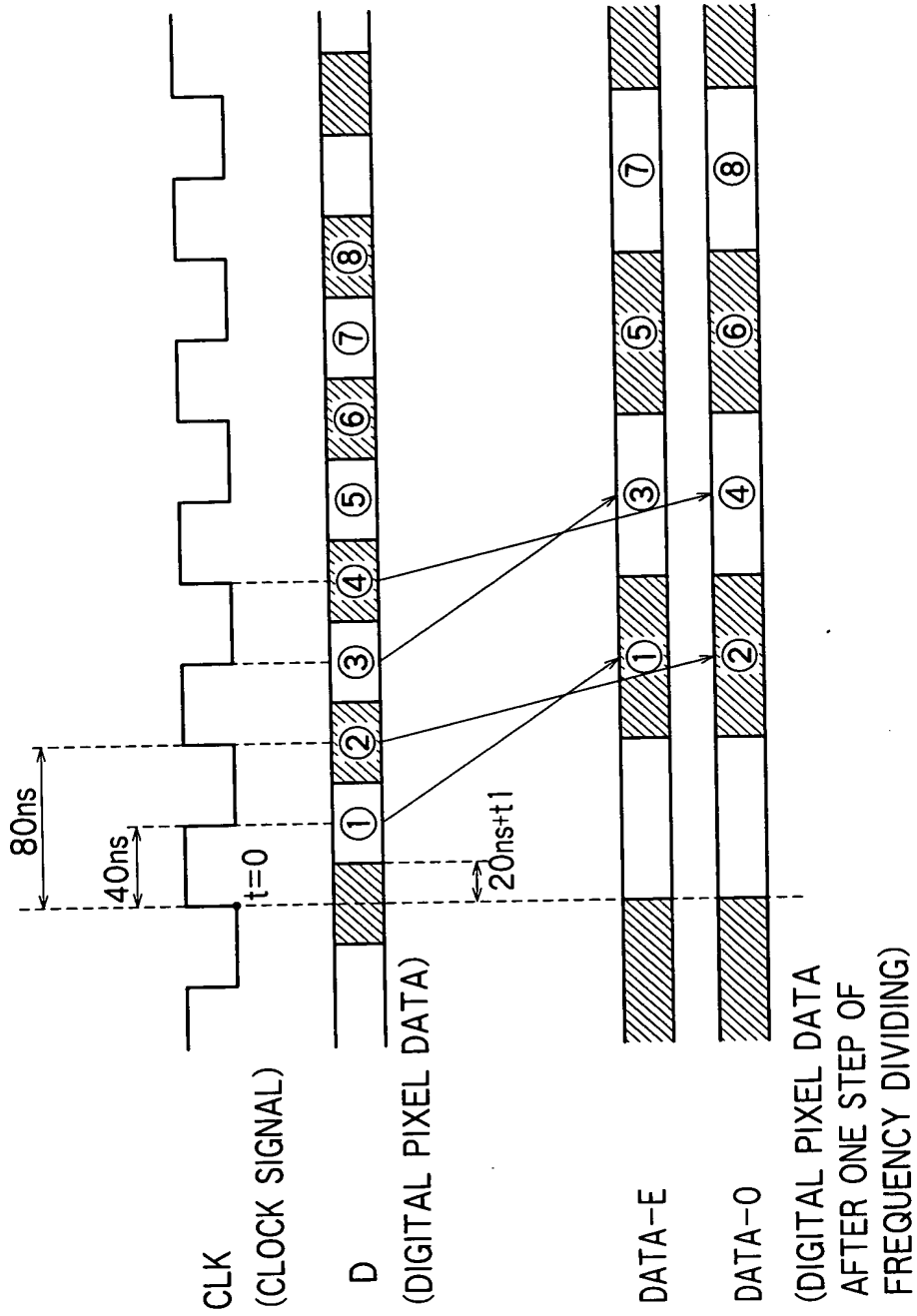


FIG. 13

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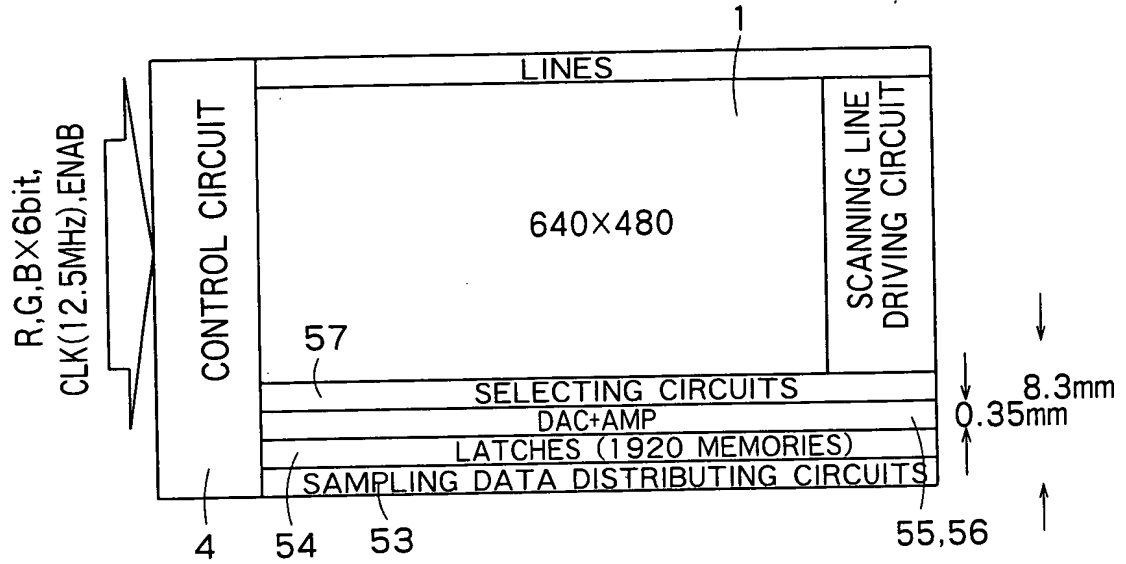


FIG. 14

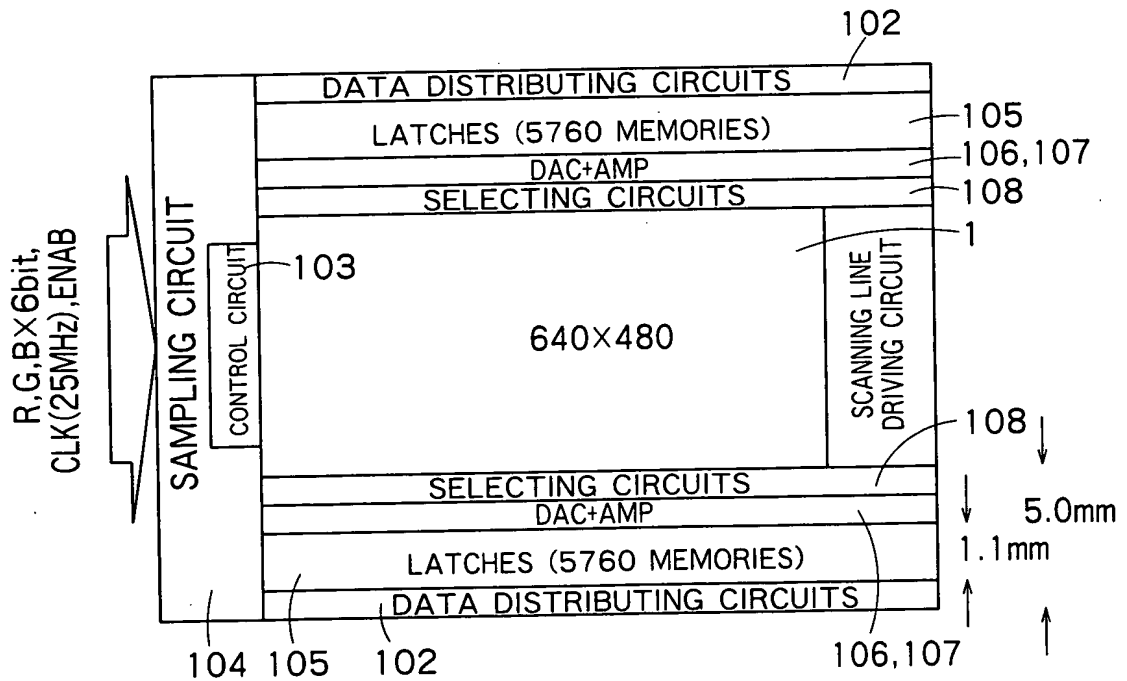


FIG. 15

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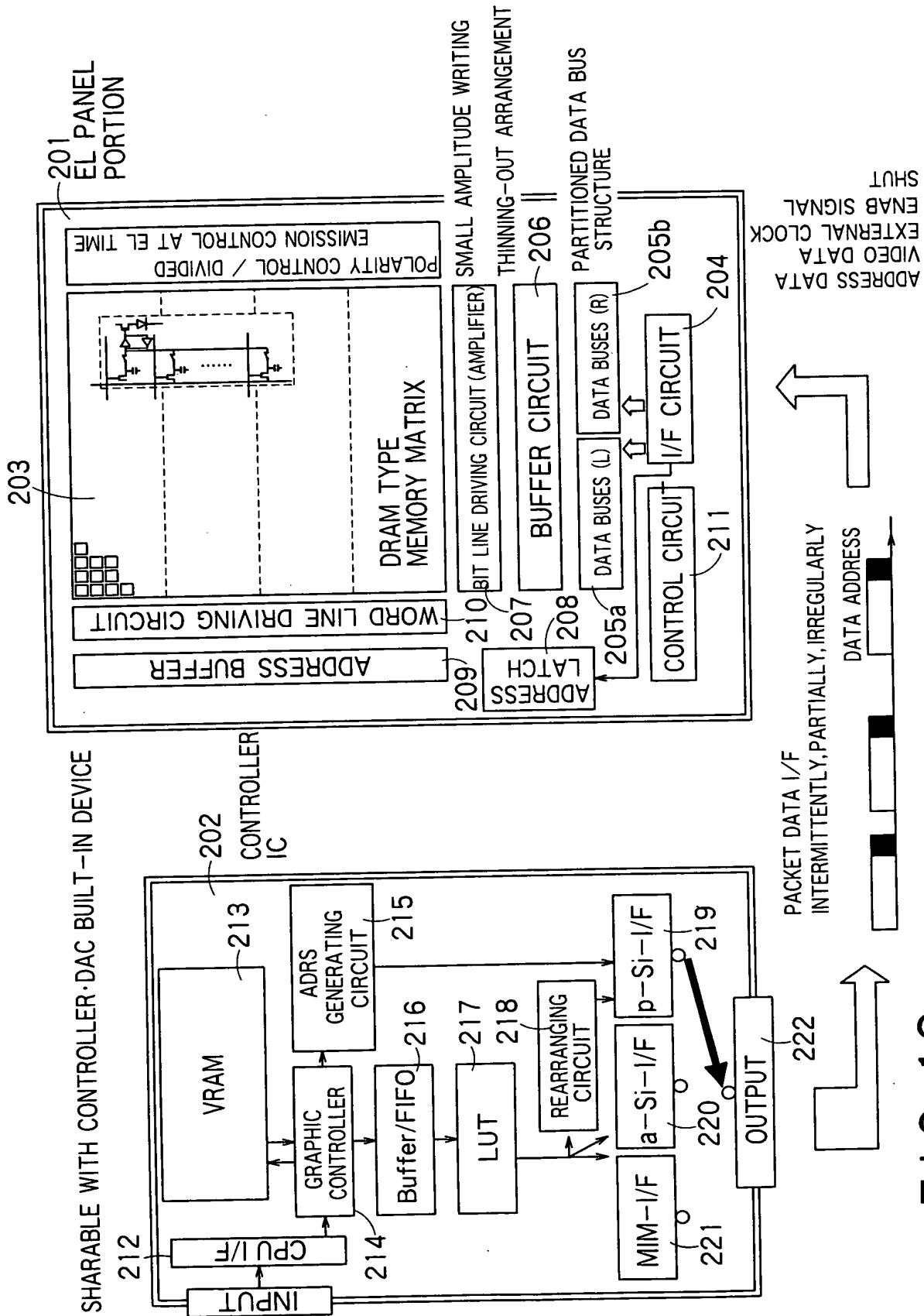


FIG. 16

FIG. 17

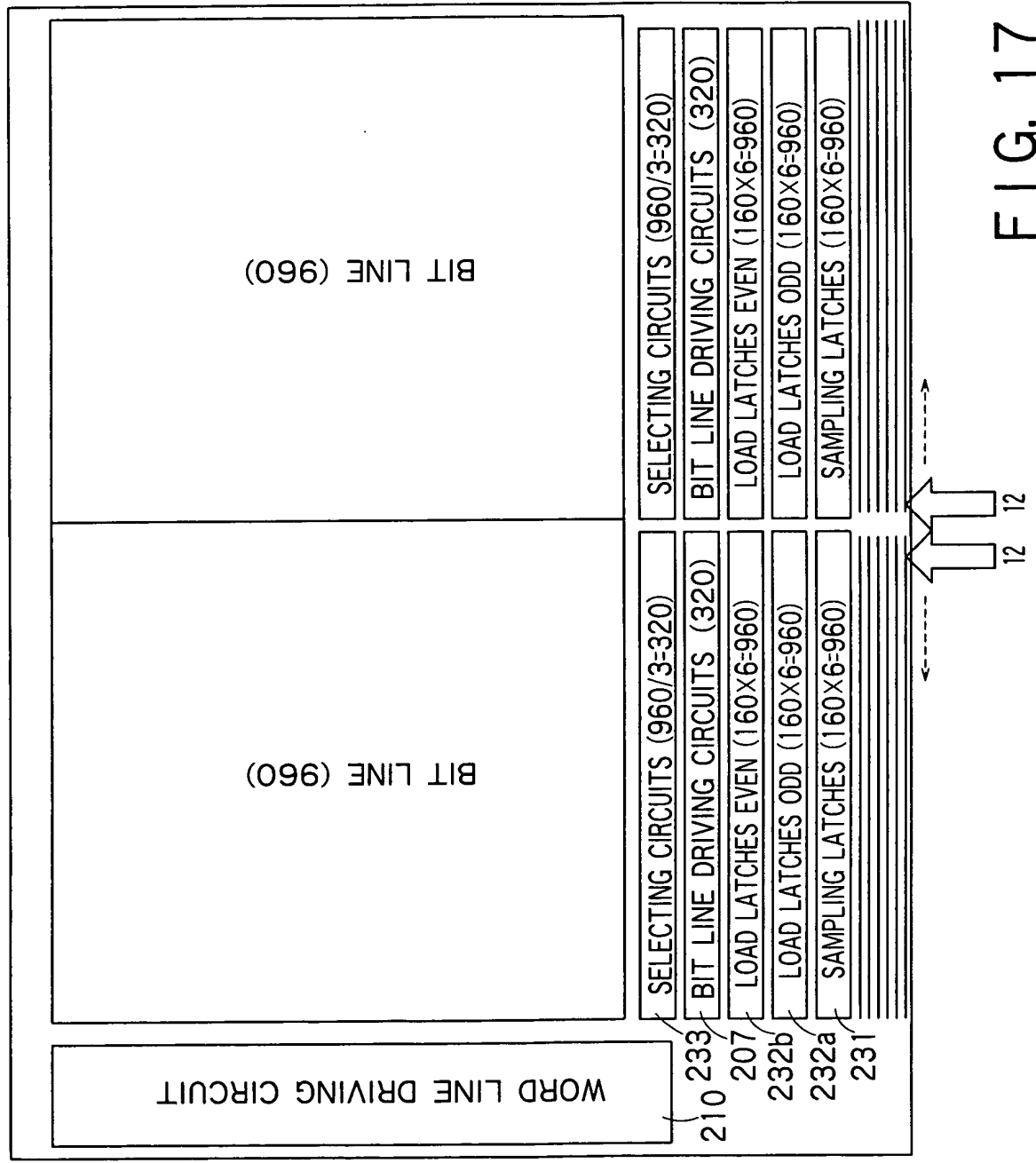


FIG. 17

[illegible]

DATA-[5:0]R1	R5	R9	R13	...	R305R309R313R317BLK	R2	R6	R10	R14	...	R306R310R314R318
DATA-[5:0]R3	R7	R11	R15	...	R307R311R315R319BLK	R4	R8	R12	R16	...	R308R312R316R320
DATA-[5:0]R637R633R629R625	...	R333R329R325R321BLK	R638R634R630R626	...	R334R330R326R322	...	R335R331R327R323BLK	R640R636R632R628	...	R336R332R328R324	

~~G1 G5 G9 G13 ... G305G309G313G317BLK G2 G6 G10 G14 ... G306G310G314G318
 G3 G7 G11 G15 ... G307G311G315G319BLK G4 G8 G12 G16 ... G308G312G316G320
 G637G633G629G625 ... G333G329G325G321BLK G638G634G630G626 ... G334G330G326G322
 G639G635G631G627 ... G335G331G327G323BLK G640G636G632G628 ... G336G332G328G324
 BLANKING
 PERIOD~~

~~B1 B5 B9 B13 ... B305B309B313B317BLK B2 B6 B10 B14 ... B306B310B314B318~~
~~B3 B7 B11 B15 ... B307B311B315B319BLK B4 B8 B12 B16 ... B308B312B316B320~~
 B637B633B629B625 ... B333B329B325B321BLK B638B634B630B626 ... B334B330B326B322
 B639B635B631B627 ... B335B331B327B323BLK B640B636B632B628 ... B336B332B328B324
 BLANKING
 PERIOD

F | G | 18

CLK./CLK(8MHz)

DATA-a,b,c,d[5:0]

ENAB./ENAB

SHUT

(POL1,POL2)

HORIZONTAL TIMING

DATA
-a,b,c,d[5:0]

CLK./CLK(8MHz)

ENAB./ENAB

TIMING CONTROL SIGNAL OF DAC ON GLASS SUBSTRATE

FIG. 19

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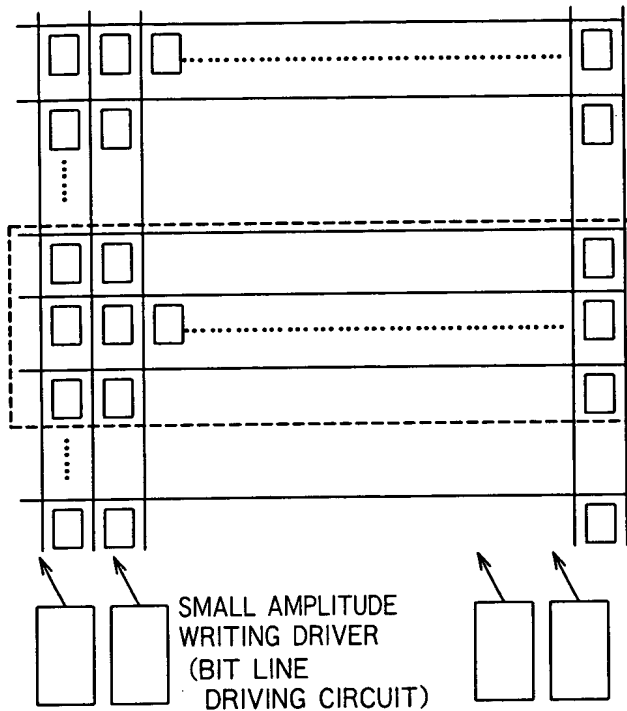


FIG. 20A

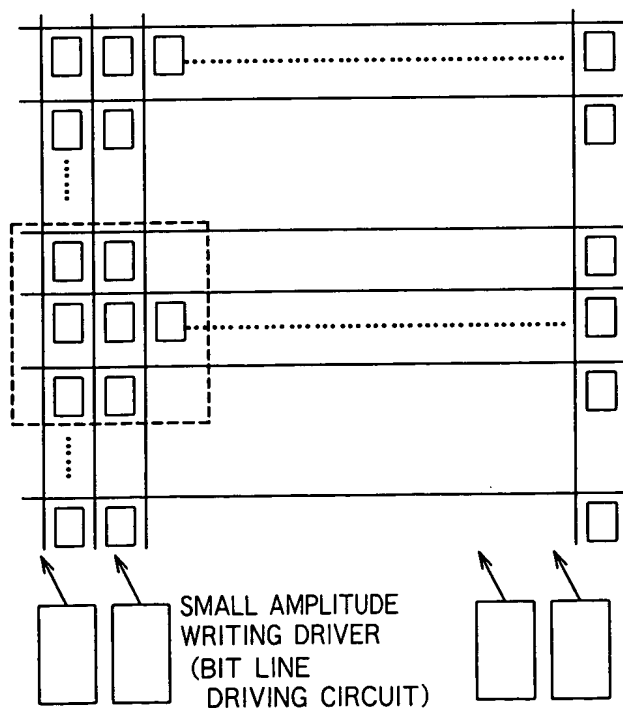


FIG. 20B

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[illegible]

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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Timing diagram for the 80CK(DATA) bus. The diagram shows a sequence of 10CK 80CK(DATA) signals. The R signal is high for odd-numbered signals and low for even-numbered signals. The G signal is high for even-numbered signals and low for odd-numbered signals. The B signal is high for odd-numbered signals and low for even-numbered signals.

[illegible][illegible]

FIG. 21

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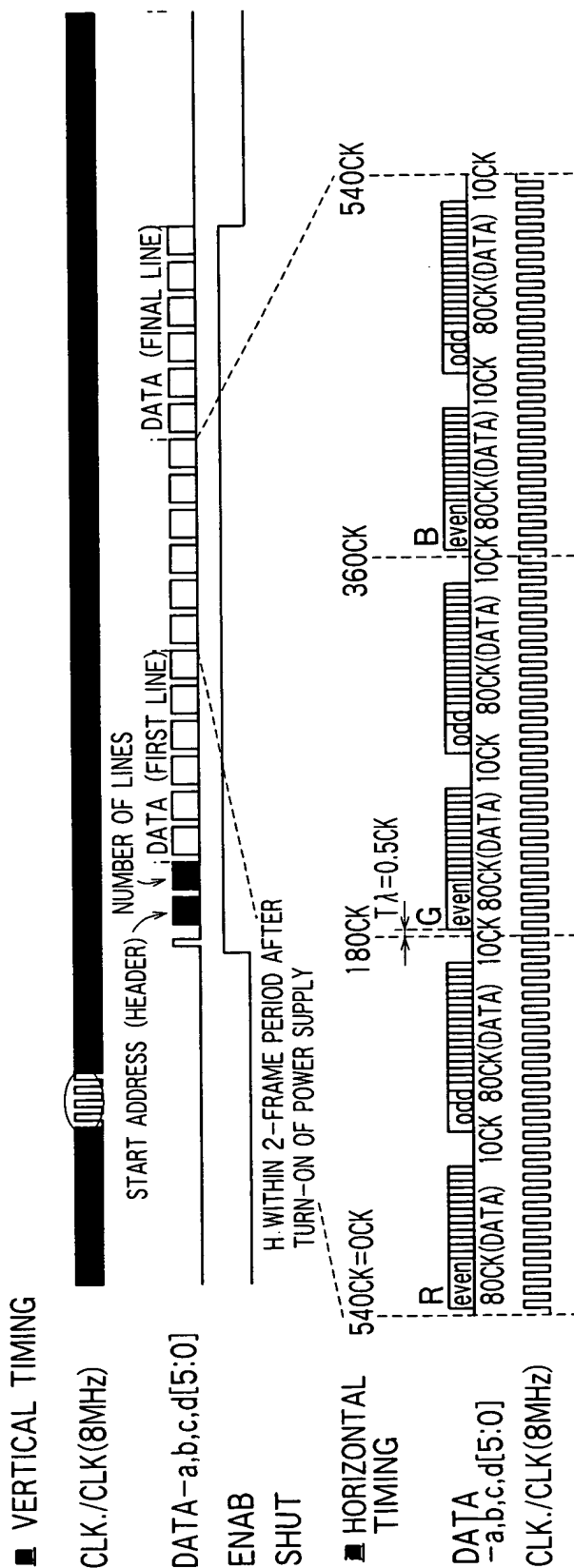


FIG. 22

CASE IN WHICH ONE DAC IS PROVIDED EVERY 6 SIGNAL LINES (1)

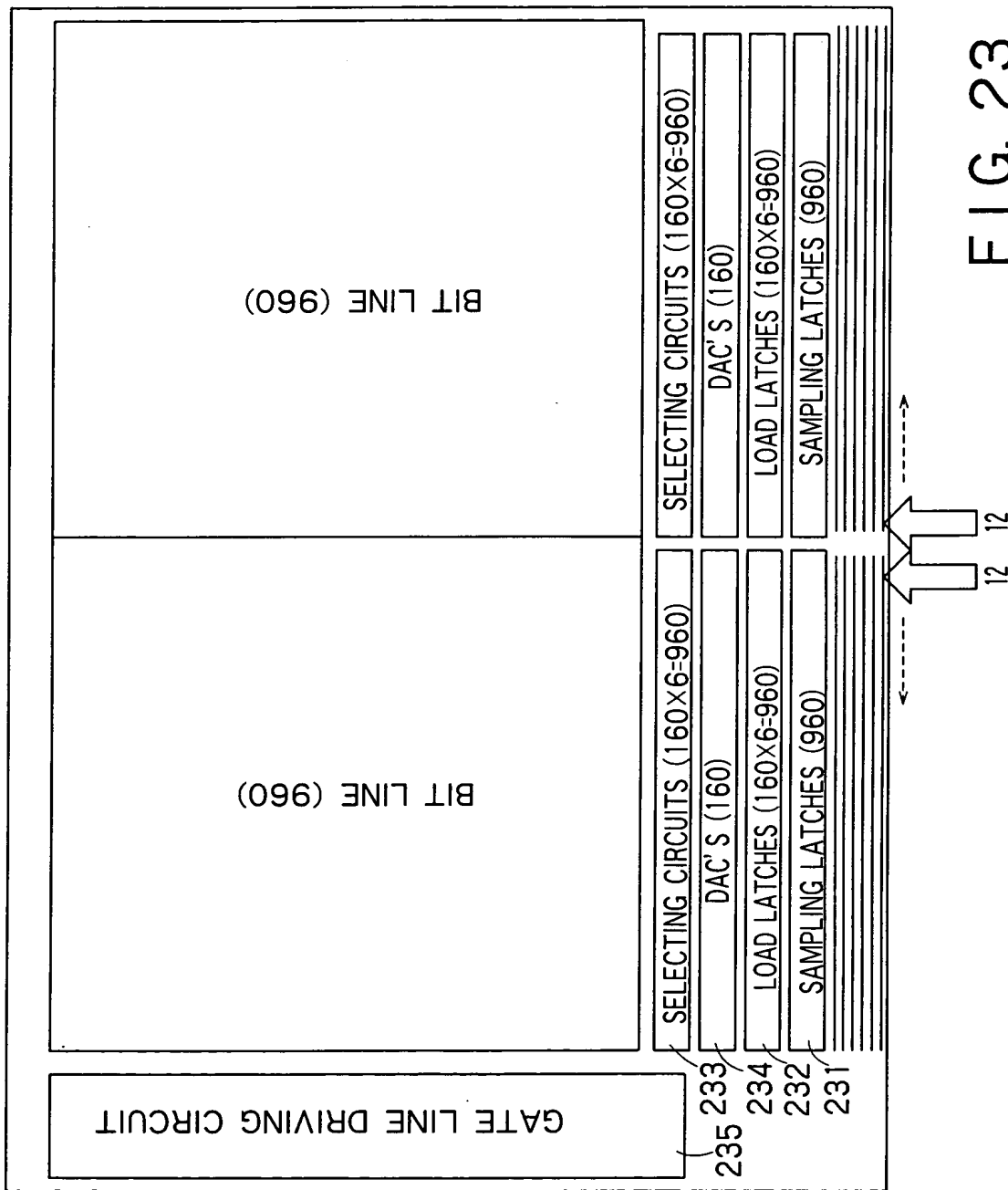


FIG. 23

CASE IN WHICH ONE DAC IS PROVIDED EVERY 3 SIGNAL LINES (1)

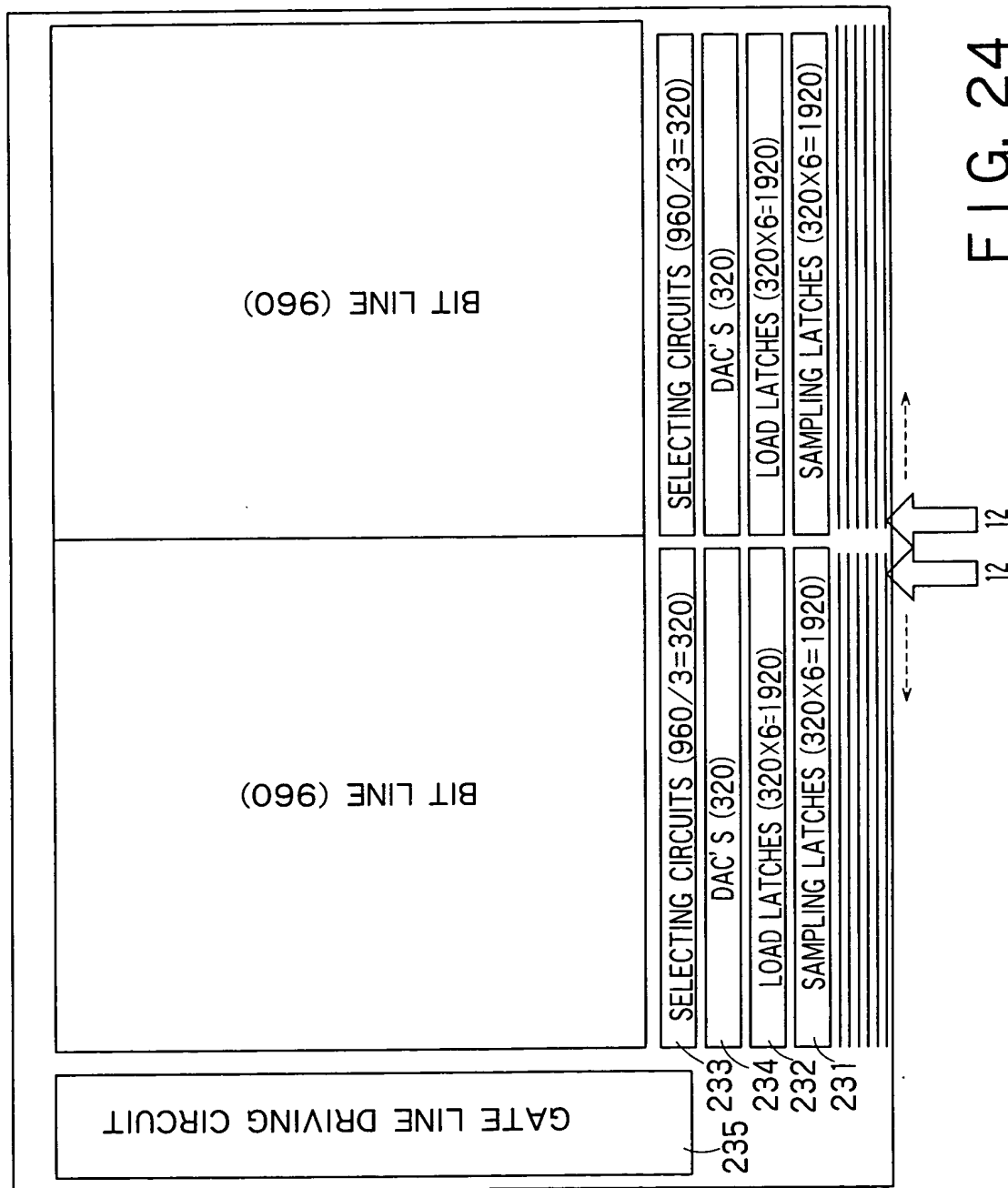


FIG. 24





FIG. 26

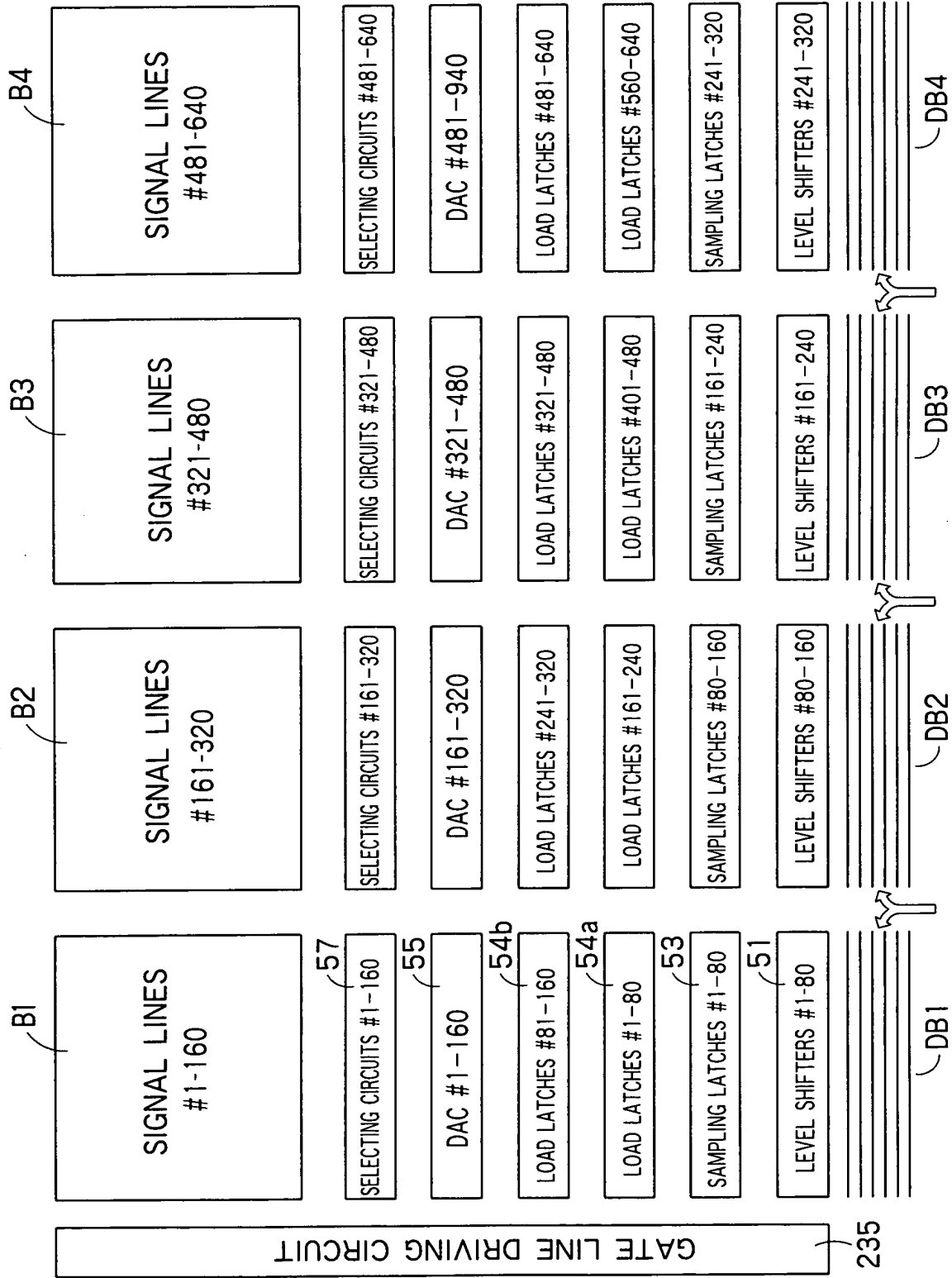


FIG. 27

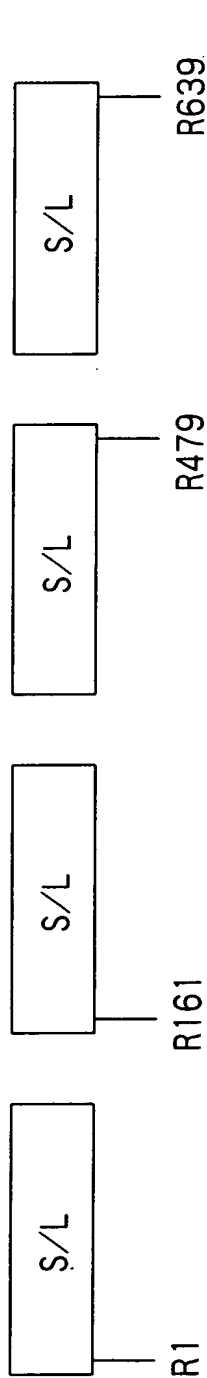


FIG. 28A

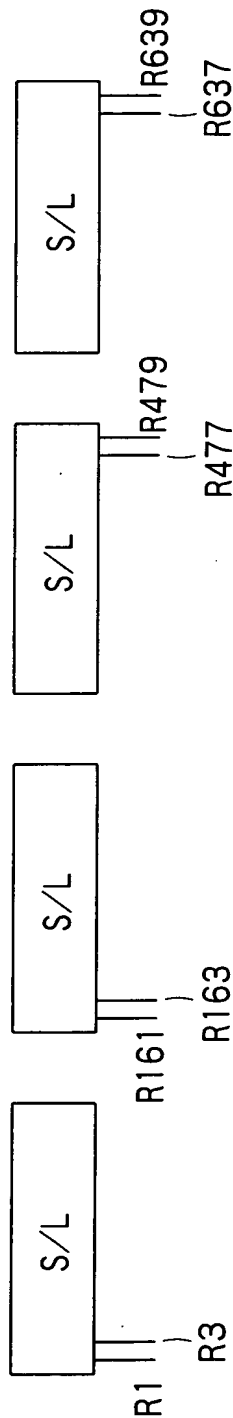


FIG. 28B

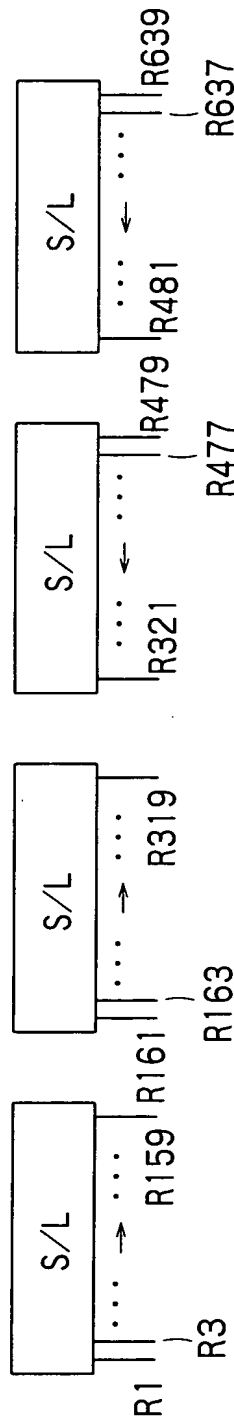


FIG. 28C

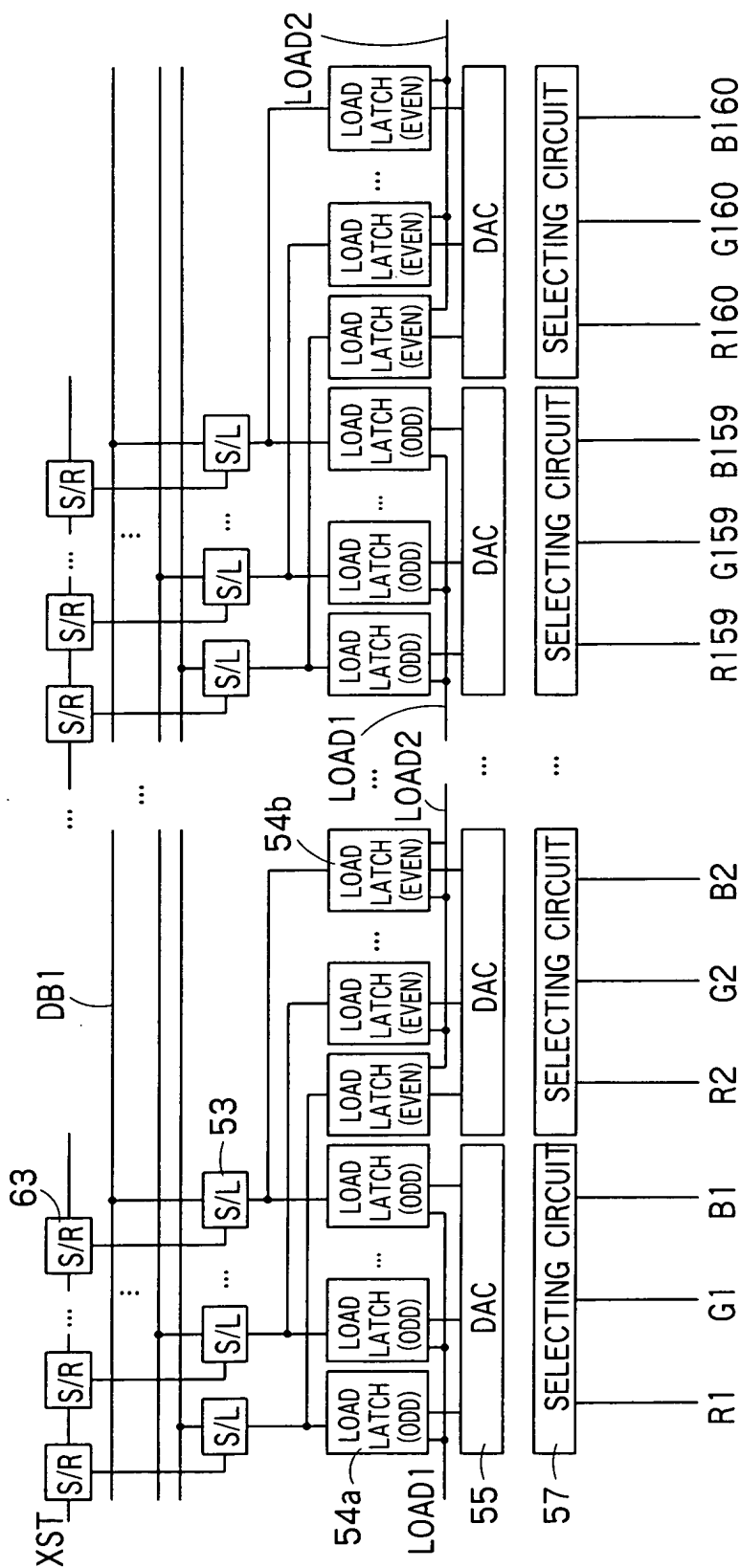


FIG. 29

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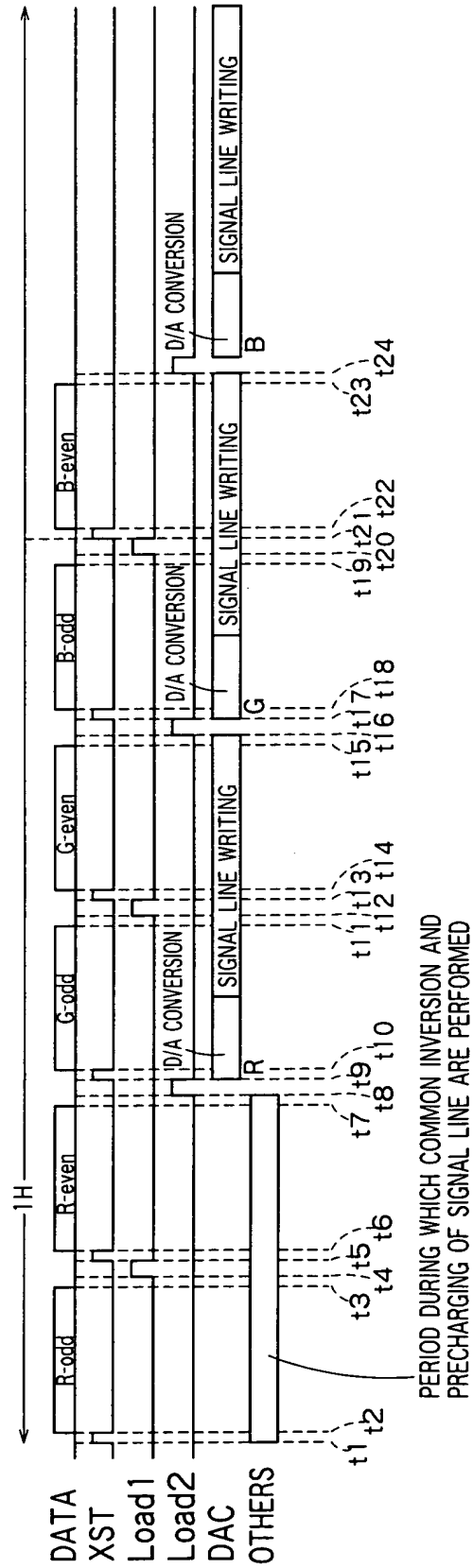


FIG. 30

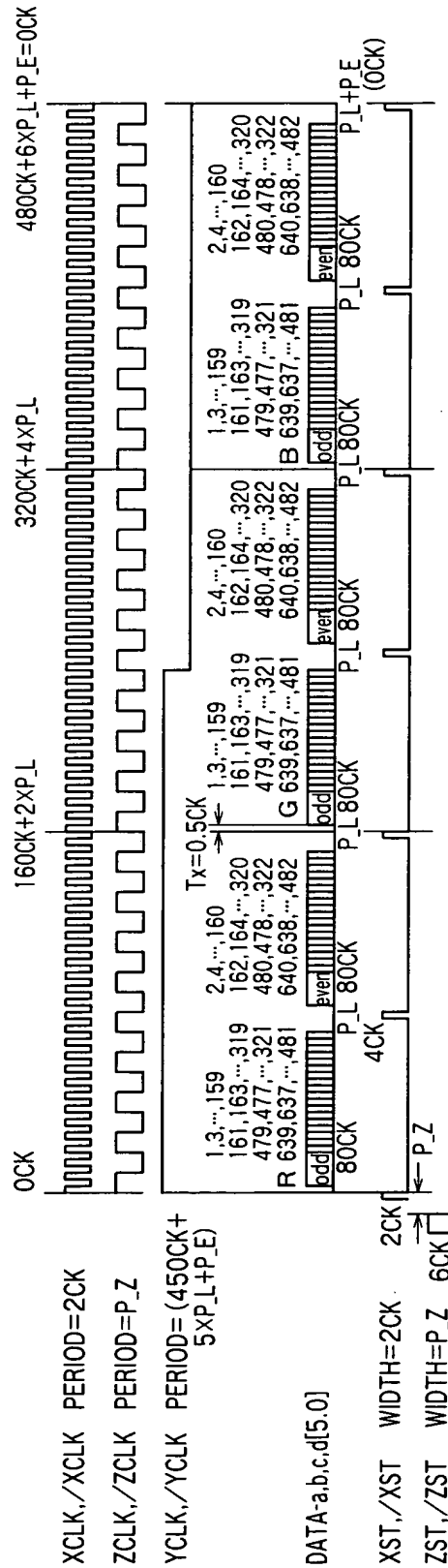


FIG. 31

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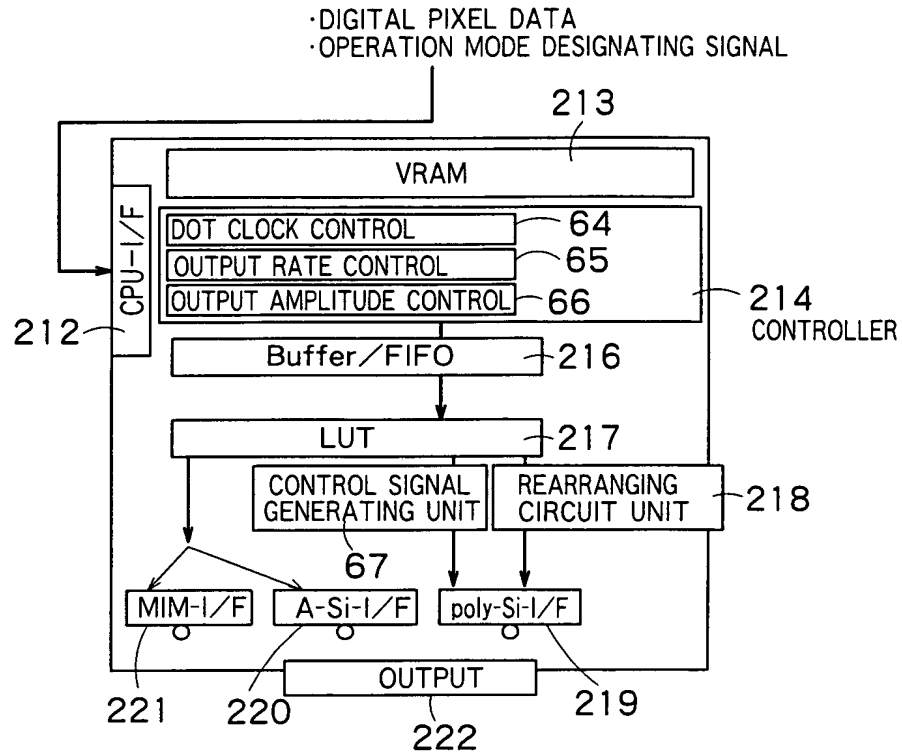


FIG. 32

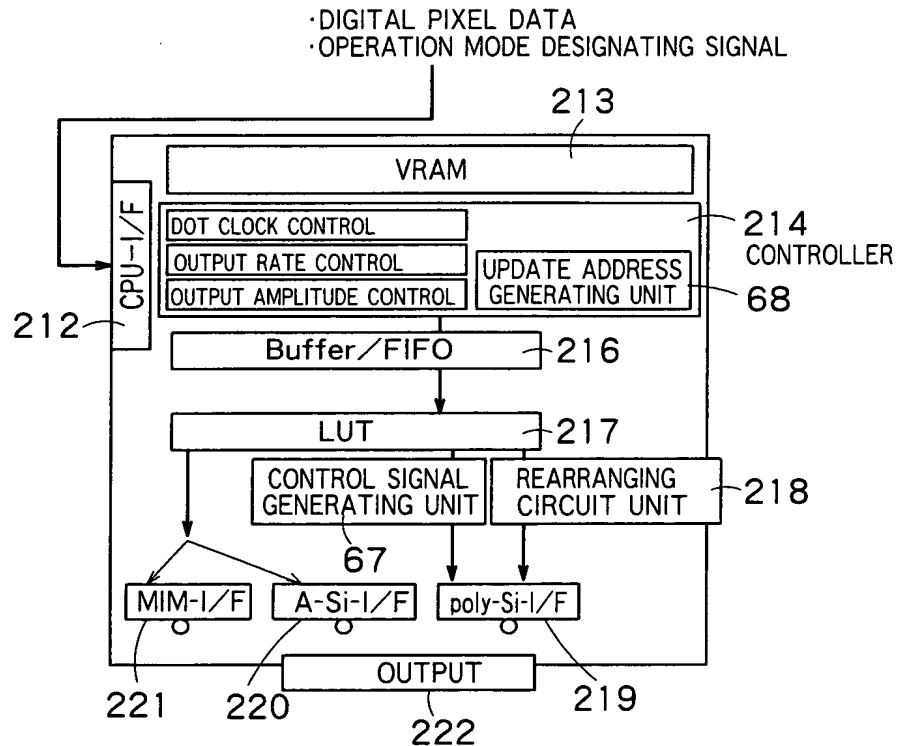


FIG. 33

TO240-00849360

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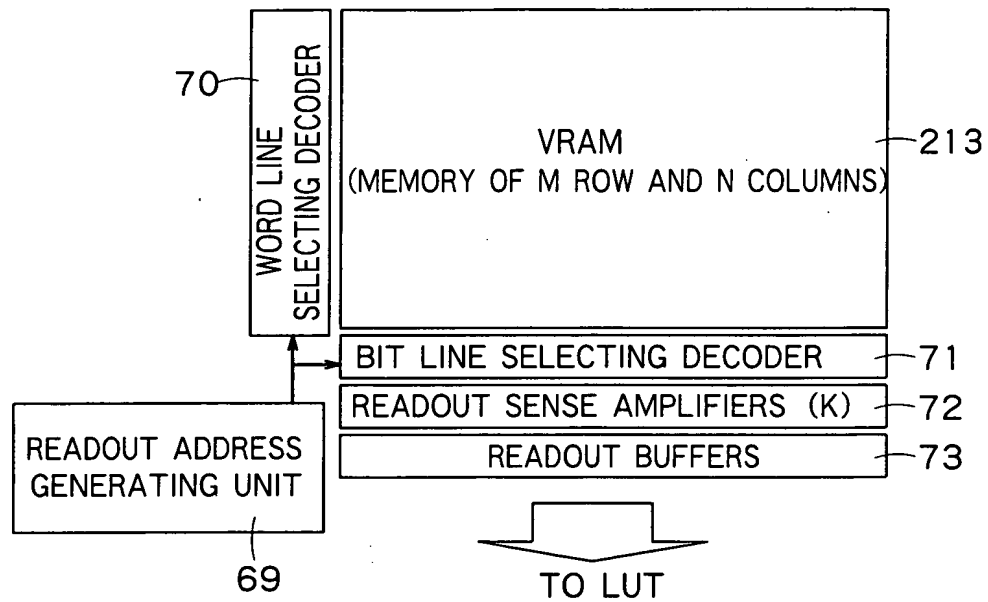


FIG. 34

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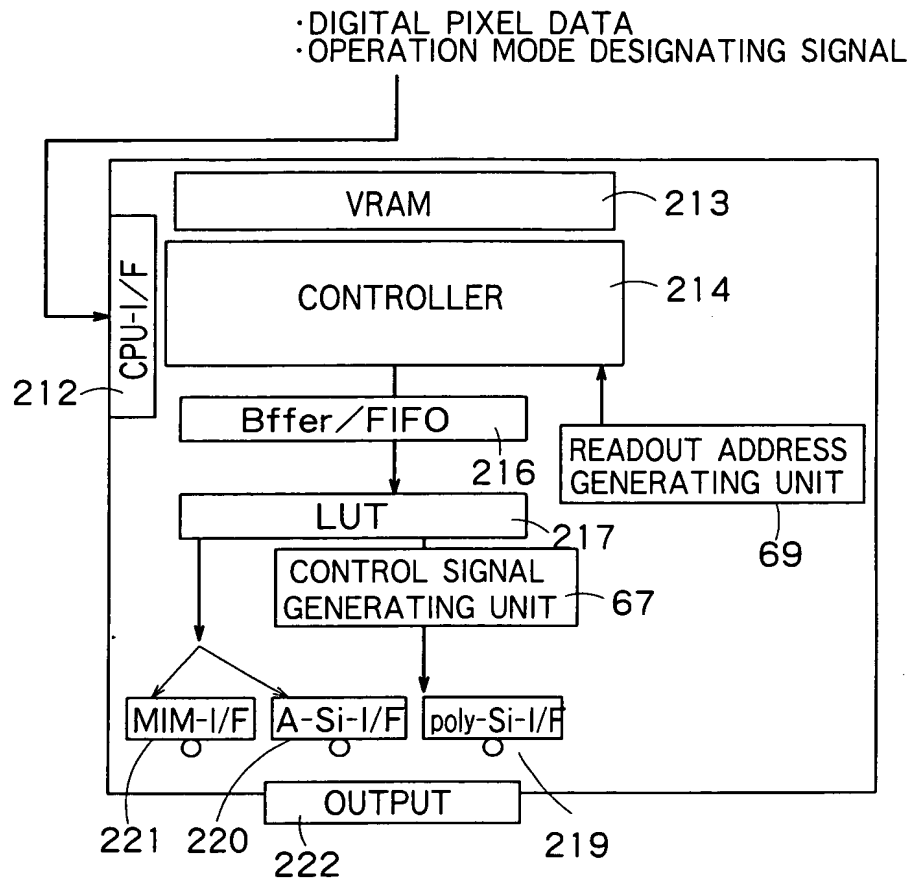


FIG. 35

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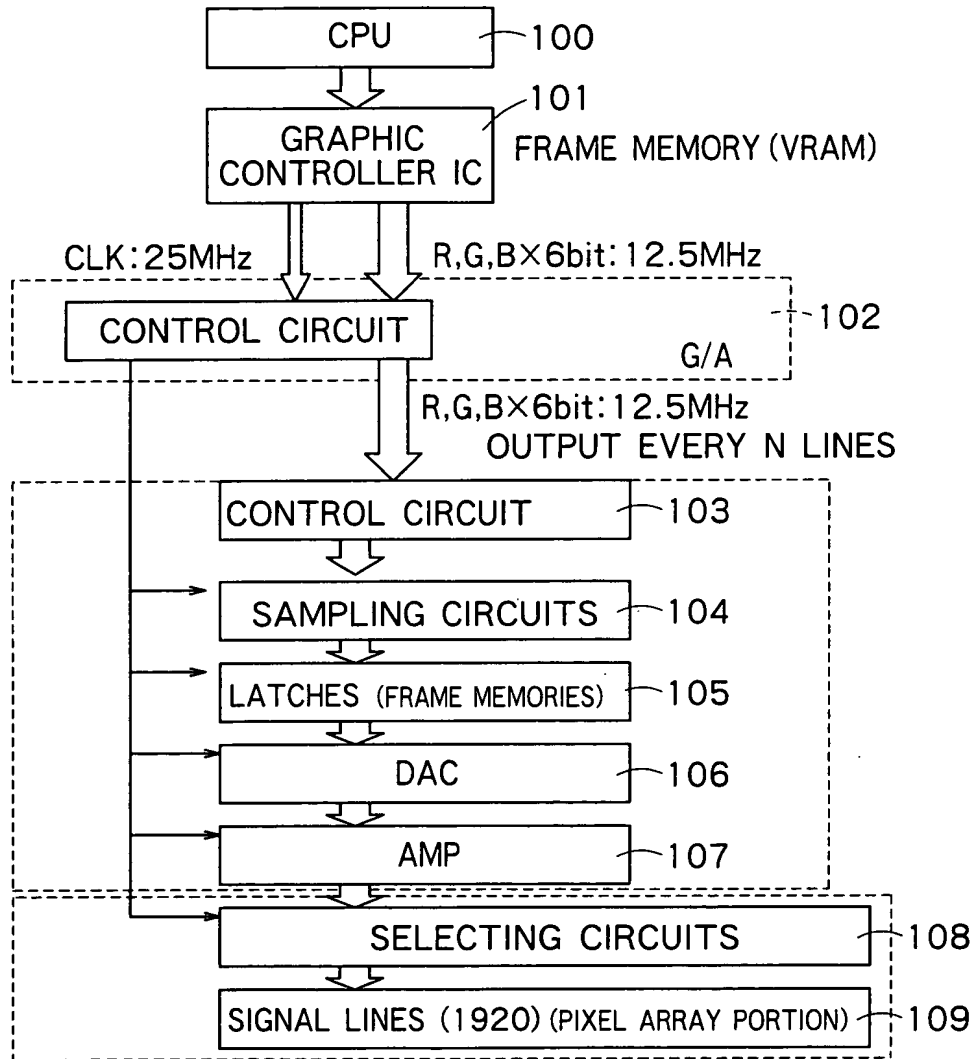


FIG. 36